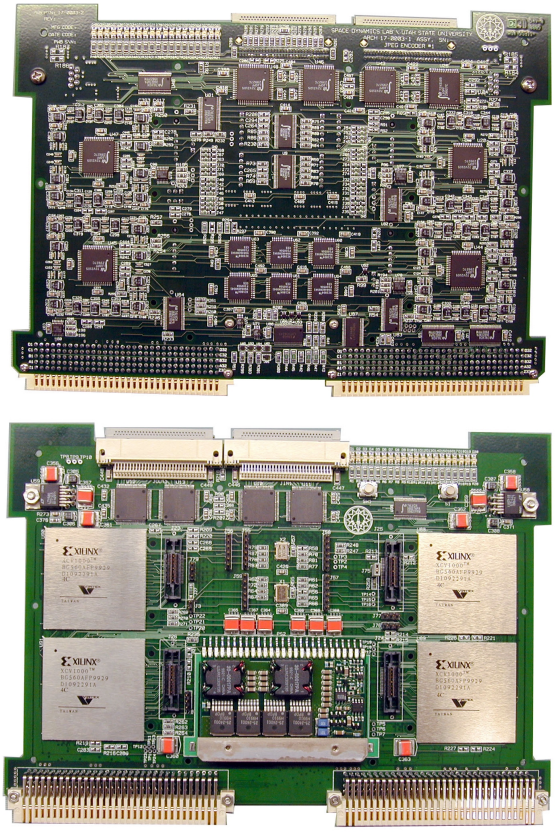
Advanced Reconnaissance Compression Hardware

Real-Time Imagery Compression for TAC/RECCE Applications

ARCH Features

- Six-card encoder set provides real-time compression:
  - 8 or 12 bit imagery
  - 2k × 2k pixels/frame at 30 frames/second
  - 5k × 5k pixels/frame at 2.5 frames/second
  - 10k × 10k pixels/frame at 1.25 frames/second
  - 12k pixels/scan at 2500 scans/second
  - 5k pixels/scan at 5000 scans/second
- Meets the National Imagery Transmission Format Standard (NITFS):
  - NITFS version 2.1
  - Joint Photographic Experts Group (JPEG) format
- Multiple interfaces, including:
  - Electro-optical/infrared (EO/IR) camera
  - Ampex Digital Cartridge Recording Systems (DCRsi)
  - Common Data Link (CDL)
  - Synthetic Aperture Radar (SAR)
- Single or dual band mode
- Built-In Test (BIT) control
- Common VME-64 interface
- Programmable compression tables
- Modular design will accommodate future higher rate single- and multi-band sensors



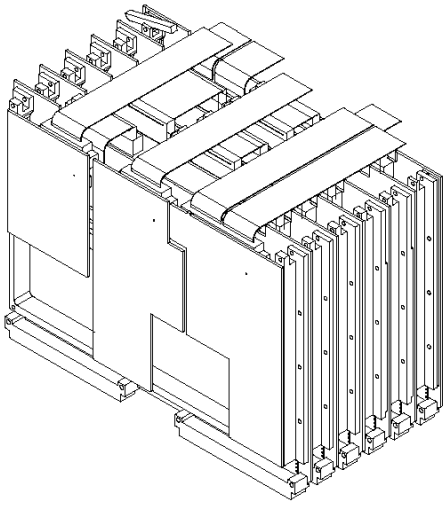
JPEG Encoder

Compression System Overview

The Space Dynamics Laboratory has developed the ARCH state-of-the-art imagery compression technology for use in next-generation reconnaissance pod systems. This system-configurable hardware set is designed to operate in the harsh TAC/RECCE platform environment and uses common hardware to provide real-time compression for many EO/IR sensor types (e.g., large format framing and scanning sensors). The ARCH JPEG compression format meets the latest NITFS requirements for TAC/RECCE imagery. ARCH provides a maximum overall data rate of 160 Mpixels/second.

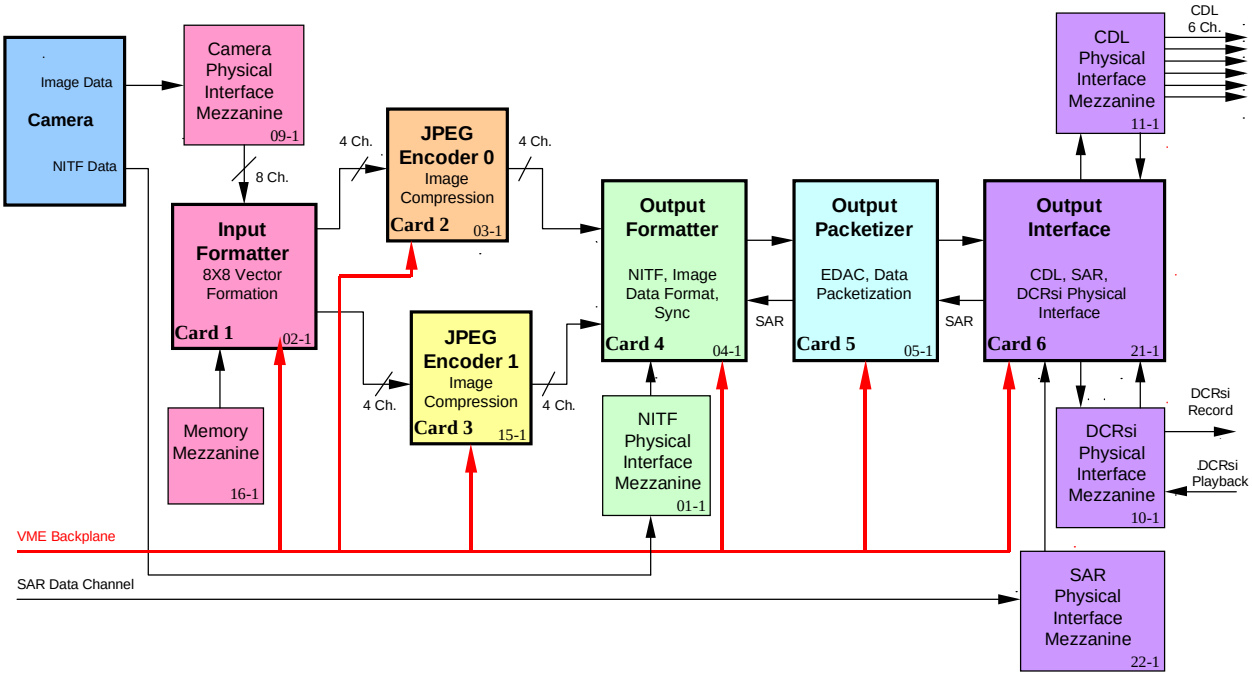
The ARCH compression system consists of a set of six formatting, compression, and interface boards: an input formatter board with camera interface and VME memory mezzanines; two JPEG compression boards; an output formatter board with NITF mezzanine; and two output interface boards, one with CDL, DCRsi, and SAR mezzanines. The ARCH receives raster frames and NITF header data from an EO/IR sensor. The image pixel data and NITF header data are received over separate channels. An input mezzanine receives the image data, while the NITF data are sent directly to an output formatter. An input formatter splits the pixel data into eight subimages along the horizontal dimension. Each subimage is then individually encoded using the JPEG algorithm. The output formatter combines the encoded subimages with the supplied NITF data, updates NITF fields where necessary, and generates an output image file. This compressed output file is then passed to a storage device and/or real-time data link. For dual-band sensors that provide alternating frames of EO and IR data, each frame is formatted as a single NITF file.

Specifications



The ARCH is based on a 10-card, conduction cooled chassis with a VME-64 back plane. The modular design utilizes mezzanine cards at significant system interfaces. The ARCH cards have been designed to allow clearance for the interface cables (camera, CDL, DCRsi, and SAR) that connect to the VME chassis. ARCH operation is controlled through the execution of C software routines. The design includes a BIT that utilizes a 512×512 test image loaded via the VME. The BIT performs data analysis and channel comparison to verify system operational status. Error and status signals are also read over the VME bus.

The input formatter card (P/N 17-0002) utilizes LVDS channel link I/O busses and has an input rate of 132-160 Mpixels/second. This card can be configured for different pixel data formats and uses two configurable lookup tables for vector processing. The card is designed for VME computer bus control/monitoring and conforms to the IEEE 1101.2-1992 standard. The configurable logic design supports future system enhancements. The JPEG encoder cards (P/N 17-0003 and 17-0015) use LVDS channel data I/O links. Each of these cards has four data channels, with up to 20 Mpixels/second throughput on each channel. The encoders support both 8 and 12 bit pixel formats, and can alternate between these formats without reloading the compression tables. The output formatter card (P/N 17-0004) uses an internal memory map divided into 256 segments of 64 KB each. This card includes an LVDS camera NITFS data interface (input clock rate of 33-40 MB/second), an LVDS JPEG encoder interface (receives data from 8 channels), and a TTL SAR interface (30 MB/second maximum input clock rate). The output packetizer board (P/N 17-0005) uses programmable, Mil grade components. The output interface board (P/N 17-0021) houses -2VCD and -5VDC power supplies. All devices on the output interface mezzanine boards are M38510 Mil grade parts.



ARCH Block Diagram

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